

Chapter 3

ECL Design Principles

This chapter is an introduction to general and Synergy-specific ECL circuit architectures and design principles. It provides a foundation for the next two chapters.

Circuit Architecture

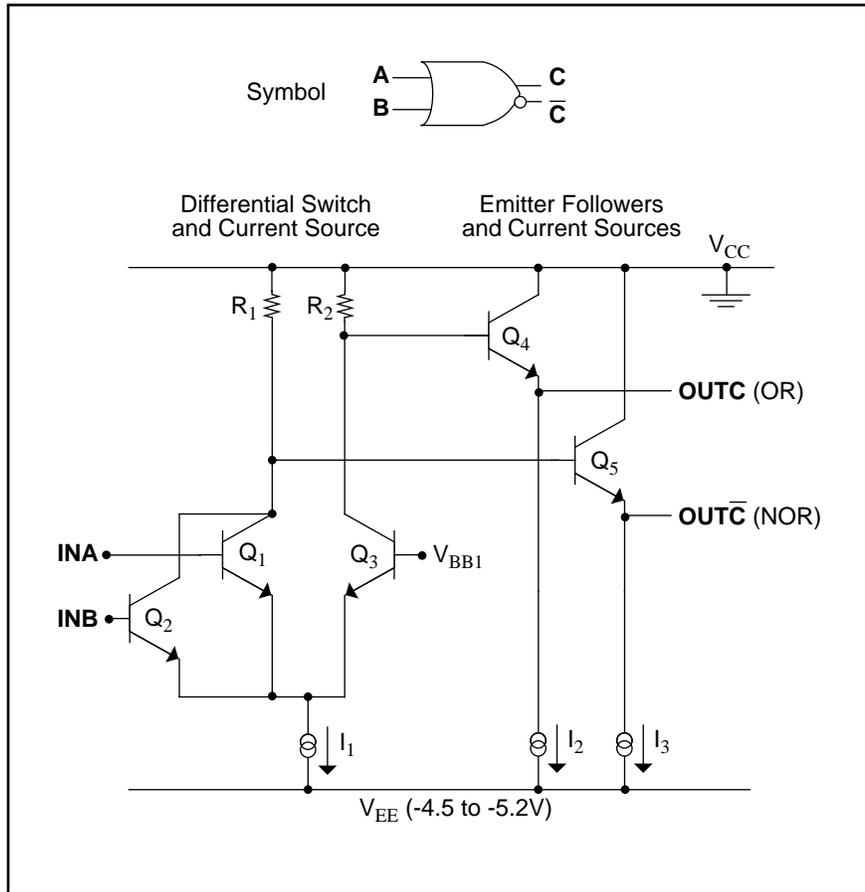
Emitter coupled logic (ECL) is a non-saturating form of digital bipolar circuit architecture. It is the fastest bipolar circuit architecture available today. In non-saturating architectures, the transistors store less charge in their bases and therefore switch much faster than saturating circuit architectures such as TTL. ECL logic can drive heavy capacitive loads or controlled-impedance transmission lines without significant effect on switching speed.

Synergy uses two-level series gating in its ECL architecture. The logic is physically implemented with *basic cells* that consist of six unconnected *npn* transistors and nine unconnected resistors. Digital functions are created from macrocell metallization patterns that use one or more contiguous basic cells.

OR-NOR Gate

Synergy's ECL logic design is based on the OR-NOR gate, shown in Figure 47. The gate consists of a differential-amplifier logic stage, with a current source, and an emitter-follower driver stage, with a separate current source. The most positive voltage (V_{cc}) is ground. The most negative voltage is V_{ee} . Current uses the standard convention; current going into a terminal is positive and current coming out is negative. The OR-NOR gate has one reference threshold level (V_{bb}) in its differential-amplifier stage, so the architecture of this particular gate is *one-level series gating*.

Figure 47. One-Level Gate (OR-NOR)



The *differential-amplifier logic stage* (or *differential switch*) consists of transistor pairs—an input transistor (Q1 or Q2) and a reference transistor (Q3)—that act as a digital switch, and a current source (I1). There are one or more transistors for each logical input, and the current source is shared by all inputs. The base of Q3 is connected to a reference voltage (V_{bb1}) which has a value between V_{cc} and V_{ee} (typically -1.3 Volts, midway between the logic-0 and logic-1 thresholds). Current always flows through the differential switch; the path taken by the current determines the output state of the switch.

The *emitter-follower driver stage* consists of transistors Q4 and Q5, and current sources I2 and I3. In this OR-NOR gate, there is one emitter-follower transistor and one current source for each logical output.

The *current sources* for the differential amplifier and the emitter-followers consist of a transistor and resistor. The transistors for all current sources have a regulated base voltage (V_{cs}), not shown in the figure, called a *bias voltage*.

All logic macrocells have one current source for each output and a separate current source for the differential switch. Some macrocells use more than one differential switch. Some macrocells have more than one emitter-follower transistor for each output, with the emitter-followers wire-ORed and using the same current source.

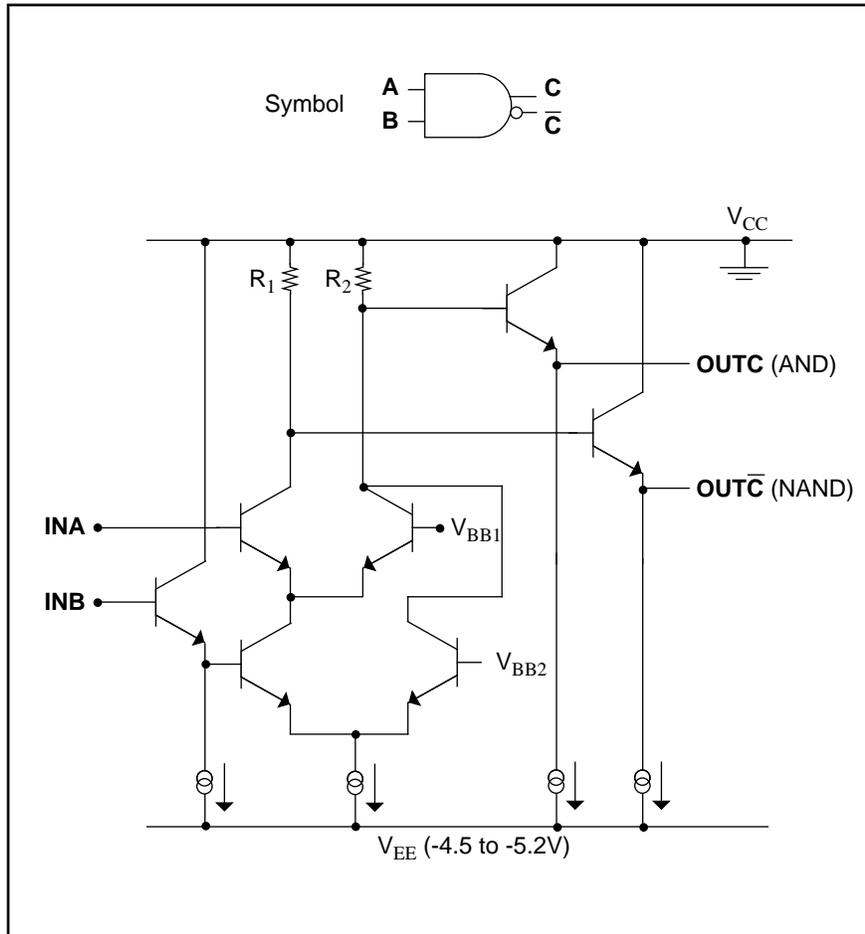
The OR-NOR gate works as follows: Q1 and/or Q2 are turned *on* by applying a high input (typically at -0.9 Volts) to their base. They are turned *off* by applying a low input (typically at -1.8 Volts). If either Q1 and/or Q2 is turned on, they will conduct all of the current through source I1 while Q3 conducts none, thereby turning Q3 off. As the current path through the differential switch changes, the base voltages of Q4 and Q5 change, thus changing the state of the outputs. In this example, the non-inverting output at Q4 will go high (more positive) and the inverting output at Q5 will go low (more negative).

The basic ECL circuit is usually enhanced in practice with subcircuits that change the input and output voltage levels as the power supply voltage and temperature changes. *Voltage compensation* is accomplished by providing the differential-amplifier stage with a true current source that is controlled by a voltage (V_{cs}) generated from a *bias network*. This is the same bias network that also generates the threshold-reference voltage (V_{bb1}). *Temperature compensation* is accomplished by providing a cross-coupled resistor-diode network between the collectors of the input (Q1, Q2) and threshold (Q3) transistors, and a zero temperature-coefficient regulator.

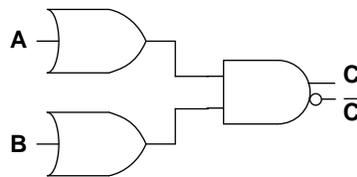
AND-NAND Gate

Most macrocells use *two-level series gating*. The AND-NAND gate is an example, shown in Figure 48. Here, the differential switch has two threshold transistors with different base voltages, V_{bb1} and V_{bb2} . The difference between the threshold voltages is equal to the base-emitter voltage of the input emitter-follower, allowing both inputs to use the same logic voltages.

Figure 48. Two-Level Gate (AND-NAND)



In ECL logic, OR gates are preferred over AND gates, and AND gates are actually built from OR gates. The two-input AND gate illustrated in the above figure can be symbolized as two single-input OR gates preceding a two-input AND gate, which is a trivial form of an OR-AND gate. In fact,



the macrocell is called a 1-1 OR-AND/NAND (the macrocell library name is OA11C) because it is logically related to the entire family of OR-AND gates.